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EXAMINER	
STIGLIC, RYAN M	
ART UNIT	PAPER NUMBER
2112	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/683,859	KELLEY ET AL.
	Examiner	Art Unit
	Ryan M. Stiglic	2112

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-32 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-32 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 10 October 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-32 are pending and have been examined.

2. Claims 1-32 are rejected.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-3 and 9-11 rejected under 35 U.S.C. 102(e) as being anticipated by Barker et al (US 20040268000A1).

For claim 1 Barker discloses:

A processor surrogate for use in a processing node of a multiprocessor data processing system having a plurality of processing nodes coupled together and to a plurality of input/output devices using corresponding communication links, the processor surrogate comprising:

- a first port comprising a first set of integrated circuit terminals adapted to be coupled to a first external communication link for coupling to one of the plurality of processing nodes (Fig. 3 and 4, item 202; [0025-0026]);
- a second port comprising a second set of integrated circuit terminals adapted to be coupled to a second external communication link for coupling to one of the plurality of input/output devices (Fig. 3 and 4, item 202; [0025-0026]); and
- an interconnection circuit coupled between said first port and said second port (Fig. 4 depicts "wiring that connects two of the point-to-point links"; [0025-0026]).

For claim 2 Barker discloses:

The processor surrogate of claim 1 wherein said interconnection circuit comprises a passive interconnection between said first port and said second port (Fig. 4; [0025-0026]).

For claim 3 Barker discloses:

The processor surrogate of claim 2 wherein said interconnection circuit further comprises:

- a first set of internal connections between a plurality of input terminals of said first port and a corresponding plurality of output terminals of said second port (Fig. 4; [0025-0026]); and
- a second set of internal connections between a plurality of input terminals of said second port and a corresponding plurality of output terminals of said first port (Fig. 4; [0025-0026]).

For claim 9 Barker discloses:

A processor surrogate for use in a multiprocessor data processing system having a first processing node including an actual processor and a second processing node coupled to the first processing node and including the processor surrogate, the processor surrogate comprising:

- an integrated circuit package having a first plurality of terminals forming a first port of the processor surrogate and disposed at locations corresponding to a first link controller of the actual processor, and a second plurality of terminals forming a second port of the processor surrogate and disposed at locations corresponding to a second link controller of the actual processor (Fig. 4; [0025-0026]); and
- a plurality of electrical connections between said first plurality of terminals of said first port and corresponding ones of said second plurality of terminals of said second port (Fig. 4; [0025-0026]).

For claim 10 Barker discloses:

The processor surrogate of claim 9 wherein said plurality of electrical connections comprises:

- a first set of internal connections between a plurality of input terminals of said first port and a corresponding plurality of output terminals of said second port (Fig. 4; [0025-0026]); and
- a second set of internal connections between a plurality of input terminals of said second port and a corresponding plurality of output terminals of said first port (Fig. 4; [0025-0026]).

For claim 11 Barker discloses:

The processor surrogate of claim 9 wherein said first and second link controllers of the actual processor are substantially compatible with the HyperTransport. I/O Link Specification, Revision 1.05 [0023,0026].

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 12 and 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barker et al. as applied to claim 9 above, and further in view of Homer et al. (US006626690B2).

Barker discloses a passive surrogate processor that allows communications to pass-through the surrogate processor directly to another connected device. In other words the surrogate processor of Barker discloses directly connecting the pins on an input side the surrogate processor to the output pins on the surrogate processor such that all signals presented to the surrogate processor on the input side are forwarded to the output side [0025-0026]. Barker discloses that when a surrogate processor is placed in a multiprocessor system two processors that were once two 'hops' away are now one 'hop' away since the surrogate processor does not consume the signals presented to it from either neighbor processor. Barker however fails to disclose directly connecting an actual processor to the memory/I/O of the surrogate processor (once actual processor).

Homer teaches a low profile jumper solution for selectively connecting various system components (Fig. 1-5). The low profile jumper solution (hereinafter multi-directional connector) is usable as a removable module of a computer system wherein system components are selectively coupled according to the orientation o the multi-directional connector (col. 5, line 22 – col. 6, line 27). The multi-directional connector of Homer allows various system devices (such as processors, memory, or I/O) to be selectively coupled to other system devices while isolating remaining system devices (col. 2, ll. 16-21; col. 2, ll. 36-38; col. 4, ll. 2-5).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to implement the multi-directional connector of Homer into the surrogate processor of Barker thus facilitating multiple switchable connections in a relatively low profile connector assembly.

For claim 12:

The processor surrogate of claim 9 wherein the multiprocessor data processing system further comprises an input/output device coupled to said second port of the processor surrogate (The invention of Barker in view of Homer provides a user with the ability to selectively connect processors to either one another or to the I/O/memory of the replaced processor by simply changing the orientation of the surrogate processor).

For claim 20:

A multiprocessor data processing system comprising:

- a first processing node comprising an actual processor (Barker; Fig. 3, 102; [0025-0026]);
- a second processing node comprising a processor surrogate having a first port coupled to said first processing node, a second port, and an interconnection circuit coupled between said first port and said second port (Barker; Fig. 3 & 4, 202; [0025-0026]); and
- an input/output device coupled to said second port of said second processing node and accessible to said actual processor via said processor surrogate (The invention of Barker in view of Homer provides a user with the ability to selectively connect processors to either one another or to the I/O/memory of the replaced processor by simply changing the orientation of the surrogate processor).

For claim 21:

The multiprocessor data processing system of claim 20 wherein said interconnection circuit comprises a passive interconnection between said first port and said second port (Barker; [0025-0026]).

For claim 22:

The multiprocessor data processing system of claim 21 wherein said interconnection circuit further comprises:

- a first set of internal connections between a plurality of input terminals of said first port and a corresponding plurality of output terminals of said second port (Barker; Fig. 4; [0025-0026]); and
- a second set of internal connections between a plurality of input terminals of said second port and a corresponding plurality of output terminals of said first port (Barker; Fig. 4; [0025-0026]).

7. Claims 1, 4-6, 9, 12-16, 19-20, 23-24, 27-32 rejected under 35 U.S.C. 103(a) as being unpatentable over Kessler et al. (US006633960B1).

For claim 1 Kessler teaches:

A processor surrogate (pass-through processor; col. 5, ll. 29-40) for use in a processing node of a multiprocessor data processing system having a plurality of processing nodes coupled together and to a plurality of input/output devices using corresponding communication links, the processor surrogate comprising:

- a first port comprising a first set of integrated circuit terminals adapted to be coupled to a first external communication link for coupling to one of the plurality of processing nodes (As shown in figures 1 and 2, processors 100 contain four ports for connecting to one of a plurality of processing nodes [N,S,E,W]. Figure 2b shows the four ports connected to router [RBOX] 200);

- a second port comprising a second set of integrated circuit terminals adapted to be coupled to a second external communication link for coupling to one of the plurality of input/output devices (Fig. 1 and 2, processors 100 contain two secondary ports for coupling input/output devices [via I/O controller 104] and memories [102]); and
- an interconnection circuit coupled between said first port and said second port (Kessler shows a router/crossbar 200 that is responsible for appropriately forwarding communication signals).

Kessler teaches a multiprocessor system comprising a plurality of processing nodes **100**. Each processing node comprises a N, S, E, and W port for communicating with an adjacent processor (Fig. 1 and 2; col. 4, line 60 – col. 5, line 14). Furthermore, each processing node possesses a port for I/O communications (col. 5, ll. 15-20) and a port for memory communications (col. 5, ll. 21-28). Kessler goes on to teach, if a physical connection is not present between a pair of processors (i.e. a processor is missing or has been removed), a bypass path is implemented using a pass-through processor (col. 5, ll. 29-40). A pass-through processor permits each processor to access a pass-through processor's (a missing processor's) memory and I/O devices (col. 5, ll. 38-39). Kessler does not expressly teach the composition of a pass-through processor however Kessler does provide one potential solution in inter-processor and I/O router unit **200** ("RBOX", col. 5, ll. 41-50). The RBOX **200** provides interfaces to as many as four other processors, an I/O controller and memory (Fig. 2b; col. 12, ll. 11-15). Therefore Kessler teaches the presence of the RBOX in a pass-through processor since the pass-through processor permits access to a processor's memory and I/O devices (col. 5, ll. 35-40; In other words since a pass-through processor communicates with adjacent processing nodes and allows them access to the pass-through processor's memory and I/O devices, much like a processing node with an RBOX, an RBOX is likely found within the pass-through processor). While Kessler does not expressly teach an RBOX within a pass-through processor one of ordinary skill in the art would recognize that the RBOX provides an easy solution to the problem of providing access to a processor's (a vacant processor's) memory and I/O devices since the RBOX permits access to processors connected on each of a N, S, E, and W port.

For claim 4 Kessler teaches:

The processor surrogate of claim 1 wherein said interconnection circuit comprises an active interconnection between said first port and said second port (Fig. 2b, RBOX **200;** col. 12, ll. 11-15).

For claim 5 Kessler teaches:

The processor surrogate of claim 4 wherein said interconnection circuit further comprises:

- a first communication link controller coupled to said first port (Fig. 2b, boxes N, S, E, W attached to router/RBOX **200**);
- a second communication link controller coupled to said second port (Fig. 2b, the box labeled IO connected to router/RBOX **200**; see also Fig. 1, 104); and
- a crossbar switch having a first terminal coupled to said first communication link controller, and a second terminal coupled to said second communication link controller

(Router/RBOX **200** acts as a crossbar switch forwarding communication signals from one port to another).

For claim 6 Kessler teaches:

The processor surrogate of claim 5 wherein said interconnection circuit further comprises:

- a memory controller coupled to said crossbar switch and adapted to be coupled to an external memory, for controlling accesses between said first and second communication link controllers and said external memory (Fig. 2b, 190; col. 5, ll. 47-50; col. 11, ll. 50-52).

For claim 9 Kessler teaches:

A processor surrogate for use in a multiprocessor data processing system having a first processing node including an actual processor and a second processing node coupled to the first processing node and including the processor surrogate, the processor surrogate comprising:

- an integrated circuit package having a first plurality of terminals forming a first port of the processor surrogate and disposed at locations corresponding to a first link controller of the actual processor, and a second plurality of terminals forming a second port of the processor surrogate and disposed at locations corresponding to a second link controller of the actual processor (As shown in figures 1 and 2, processors 100 contain four ports for connecting to one of a plurality of processing nodes [N,S,E,W] and contain two secondary ports for coupling input/output devices [via I/O controller 104] and memories [102]. Figure 2b shows the four ports connected to router [RBOX] 200); and

- a plurality of electrical connections between said first plurality of terminals of said first port and corresponding ones of said second plurality of terminals of said second port (the RBOX **200** serves as the electrical connections between the various ports).

Please see the discussion above, with respect to claim 1, regarding the particular teachings of Kessler.

For claim 12 Kessler teaches:

The processor surrogate of claim 9 wherein the multiprocessor data processing system further comprises an input/output device coupled to said second port of the processor surrogate (Fig. 1 and 2, processors 100 contain two secondary ports for coupling input/output devices [via I/O controller 104] and memories [102]).

For claim 13 Kessler teaches:

A processor surrogate for use in a multiprocessor data processing system having a plurality of processing nodes comprising a first processing node including an actual processor and a second processing node coupled to the first processing node and including the processor surrogate, the processor surrogate comprising:

- a first port comprising a first set of integrated circuit terminals adapted to be coupled to a first external communication link and thereby to one of the plurality of processing nodes (As shown in figures 1 and 2, processors 100 contain four ports for connecting to one of a plurality of processing nodes [N,S,E,W]. Figure 2b shows the four ports connected to router [RBOX] 200);

- a second port comprising a second set of integrated circuit terminals adapted to be coupled to a second external communication link and thereby to an input/output device (Fig. 1 and 2, processors 100 contain two secondary ports for coupling input/output devices [via I/O controller 104] and memories [102]); and
- an active interconnection circuit coupled between said first port and said second port to thereby couple said one of the plurality of processing nodes and said input/output device (Kessler shows a router/crossbar 200 that is responsible for appropriately forwarding communication signals).

Please see the discussion above, with respect to claim 1, regarding the particular teachings of Kessler.

For claim 14 Kessler teaches:

The processor surrogate of claim 13 wherein said one of the plurality of processing nodes comprises said first node including said actual processor (As previously discussed, Kessler teaches a surrogate processor (also known as a pass-through processor), is inserted into the multiprocessor system to allow actual processors to access the memory and I/O device of a processor that has been removed).

For claim 15 Kessler teaches:

The processor surrogate of claim 13 wherein said active interconnection circuit comprises:

- a first communication link controller coupled to said first port (Fig. 2b, boxes N, S, E, W attached to router/RBOX **200**);
- a second communication link controller coupled to said second port (Fig. 2b, the box labeled IO connected to router/RBOX **200**; see also Fig. 1, 104); and
- a crossbar switch having a first terminal coupled to said first communication link controller, and a second terminal coupled to said second communication link controller (Router/RBOX **200** acts as a crossbar switch forwarding communication signals from one port to another).

For claim 16 Kessler teaches:

The processor surrogate of claim 15 further comprising: a memory controller coupled to said crossbar switch and adapted to be coupled to an external memory, for controlling accesses between said first and second communication link controllers and said external memory (Fig. 2b, 190; col. 5, ll. 47-50; col. 11, ll. 50-52).

For claim 19 Kessler teaches:

The processor surrogate of claim 13 further comprising:

- a third port comprising a third set of integrated circuit terminals coupled to said active interconnection circuit and adapted to be coupled to a third external communication link and thereby to a second input/output device (Kessler teaches an I/O port of the processor surrogate connects to a plurality of I/O devices **105 and 106**. While Kessler may only expressly teach the use of one I/O port connected to the RBOX, one of ordinary skill in the art would be able to easily modify the invention of Kessler such that an additional I/O port is added to provide additional I/O devices, thus increasing the connectivity of the multiprocessor system).

For claim 20 Kessler teaches:

A multiprocessor data processing system (Fig. 1, 90) comprising:

- a first processing node comprising an actual processor (Fig. 1, 100);
- a second processing node comprising a processor surrogate (pass-through processor; col. 5, ll. 29-40) having a first port coupled to said first processing node (As shown in figures 1 and 2, processors 100 contain four ports for connecting to one of a plurality of processing nodes [N,S,E,W]. Figure 2b shows the four ports connected to router [RBOX] 200), a second port (Fig. 1 and 2, processors 100 contain two secondary ports for coupling input/output devices [via I/O controller 104] and memories [102]), and an interconnection circuit coupled between said first port and said second port (Kessler shows a router/crossbar 200 that is responsible for appropriately forwarding communication signals); and
- an input/output device coupled to said second port of said second processing node and accessible to said actual processor via said processor surrogate (Kessler shows a router/crossbar 200 that is responsible for appropriately forwarding communication signals to the I/O controller **104** and I/O devices **105 and 106**).

Please see the discussion above, with respect to claim 1, regarding the particular teachings of Kessler.

For claim 23 Kessler teaches:

The multiprocessor data processing system of claim 20 wherein said interconnection circuit comprises an active interconnection between said first port and said second port (Fig. 2b, RBOX **200;** col. 12, ll. 11-15).

For claim 24 Kessler teaches:

The multiprocessor data processing system of claim 23 wherein said interconnection circuit further comprises:

- a first communication link controller coupled to said first port (Fig. 2b, boxes N, S, E, W attached to router/RBOX **200**);
- a second communication link controller coupled to said second port (Fig. 2b, the box labeled IO connected to router/RBOX **200**; see also Fig. 1, 104); and
- a crossbar switch having a first terminal coupled to said first communication link controller, and a second terminal coupled to said second communication link controller (Router/RBOX **200** acts as a crossbar switch forwarding communication signals from one port to another).

For claim 27 Kessler teaches:

The multiprocessor data processing system of claim 24 further comprising:

- a memory controller coupled to said crossbar switch and adapted to be coupled to an external memory, for controlling accesses between said first and second communication link controllers and said external memory (Fig. 2b, 190; col. 5, ll. 47-50; col. 11, ll. 50-52).

For claim 28 Kessler teaches:

A multiprocessor data processing system comprising:

- a first processing node comprising an actual processor (Fig. 1, 100);
- a second processing node comprising a first processor surrogate (pass-through processor; col. 5, ll. 29-40) having a first port coupled to said first processing node (As shown in figures 1 and 2, processors 100 contain four ports for connecting to one of a plurality of processing nodes [N,S,E,W]. Figure 2b shows the four ports connected to router [RBOX] 200), a second port (Fig. 1 and 2, processors 100 contain two secondary ports for coupling input/output devices [via I/O controller 104] and memories [102]), a third port (As shown in figures 1 and 2, processors 100 contain four ports for connecting to one of a plurality of processing nodes [N,S,E,W]. Figure 2b shows the four ports connected to router [RBOX] 200), and an interconnection circuit coupled between said first port, said second port, and said third port (Kessler shows a router/crossbar 200 that is responsible for appropriately forwarding communication signals);
- a third processing node coupled to said third port of said first processor surrogate in said second processing node (Fig. 1, processors 100 are connected to 4 adjacent actual processing nodes or pass-through processors);

- a fourth processing node coupled to said third processing node and to said first processing node (Fig. 1, processors 100 are connected to 4 adjacent actual processing nodes or pass-through processors); and
- a first input/output device coupled to said second port of said second processing node and accessible to said actual processor via said first processor surrogate (Kessler shows a router/crossbar 200 that is responsible for appropriately forwarding communication signals to the I/O controller **104** and I/O devices **105 and 106**).

Please see the discussion above, with respect to claim 1, regarding the particular teachings of Kessler.

For claim 29 Kessler teaches:

The multiprocessor data processing system of claim 28 wherein said third processing node comprises a second processor surrogate (pass-through processor; col. 5, ll. 29-40; Fig. 1, processors 100 are connected to 4 adjacent actual processing nodes or pass-through processors) having a first port coupled to said third port of said first processor surrogate in said second processing node (As shown in figures 1 and 2, processors 100 contain four ports for connecting to one of a plurality of processing nodes [N,S,E,W]. Figure 2b shows the four ports connected to router [RBOX] 200), a second port (Fig. 1 and 2, processors 100 contain two secondary ports for coupling input/output devices [via I/O controller 104] and memories [102]), a third port coupled to said fourth processing node (As shown in figures 1 and 2, processors 100 contain four ports for connecting to one of a plurality of processing nodes [N,S,E,W]. Figure 2b shows the four ports connected to router [RBOX] 200), and an interconnection circuit coupled between said first port, said second port, and said third port thereof (Kessler shows a router/crossbar 200 that is responsible for appropriately forwarding communication signals).

Please see the discussion above, with respect to claim 1, regarding the particular teachings of Kessler.

For claim 30 Kessler teaches:

The multiprocessor data processing system of claim 29 further comprising:

- a second input/output device coupled to said second port of said second processor surrogate and accessible to said actual processor via said first processor surrogate and said second processor surrogate (Kessler shows a router/crossbar 200 that is responsible for appropriately forwarding communication signals to the I/O controller **104** and I/O devices **105 and 106**).

Please see the discussion above, with respect to claim 1, regarding the particular teachings of Kessler.

For claim 31 Kessler teaches:

The multiprocessor data processing system of claim 30 wherein said fourth processing node comprises a third processor surrogate (pass-through processor; col. 5, ll. 29-40; Fig. 1, processors 100 are connected to 4 adjacent actual processing nodes or pass-through processors) having a first port coupled to said third processing node (As shown in figures 1 and 2, processors 100 contain four ports for connecting to one of a plurality of processing nodes [N,S,E,W]. Figure 2b shows the four ports connected to router [RBOX] 200), a second port (Fig. 1 and 2, processors 100 contain two secondary ports for coupling input/output devices [via I/O controller 104] and memories [102]), a third port coupled to said first processing node (As shown in figures 1 and 2, processors 100 contain four ports for connecting to one of a plurality of processing nodes [N,S,E,W]. Figure 2b shows the four ports connected to router [RBOX] 200), and an interconnection circuit coupled between said first port, said second port, and said third port thereof (Kessler shows a router/crossbar 200 that is responsible for appropriately forwarding communication signals).

Please see the discussion above, with respect to claim 1, regarding the particular teachings of Kessler.

For claim 32 Kessler teaches:

The multiprocessor data processing system of claim 31 further comprising:

- a third input/output device coupled to said second port of said third processor surrogate and accessible to said actual processor via said third processor surrogate (Kessler shows a router/crossbar 200 that is responsible for appropriately forwarding communication signals to the I/O controller **104** and I/O devices **105 and 106**).

Please see the discussion above, with respect to claim 1, regarding the particular teachings of Kessler.

8. Claims 7-8, 11, 17-18, and 25-26 rejected under 35 U.S.C. 103(a) as being unpatentable over Kessler as applied to claim 5, 9, 15, and 24 above, and further in view of the HyperTransport™ I/O Link Specification.

As discussed above, Kessler teaches a multiprocessor system comprising a plurality of processing nodes **100**. Each processing node comprises a N, S, E, and W port for communicating with an adjacent processor (Fig. 1 and 2; col. 4, line 60 – col. 5, line 14). Furthermore, each processing node possesses a port for I/O communications (col. 5, ll. 15-20) and a port for memory communications (col. 5, ll. 21-28). Kessler goes on to teach, if a physical connection is not present between a pair of processors (i.e. a processor is missing or has been removed), a bypass path is implemented using a pass-through processor (col. 5, ll. 29-40). A pass-through processor permits each processor to access a pass-through processor's (a missing processor's) memory and I/O devices (col. 5, ll. 38-39). Kessler however fails to teach the communication link controller are substantially compatible with the HyperTransport™ I/O Link Specification.

The HyperTransport link is designed to deliver a high-performance and scalable interconnect between CPU, memory, and I/O devices. The HyperTransport link uses low swing differential signaling with on-die differential termination to achieve very high data rates. The HyperTransport link uses scalable frequency and data width to achieve scalable bandwidth.

HyperTransport technology provides significantly more bandwidth than current technologies, uses low-latency responses and low pin counts, and supports legacy PC buses. It is also designed to be extensible to new systems network architecture (SNA) buses, transparent to operating systems, and has little or no impact on peripheral drivers.

HyperTransport technology is designed for use in networking, telecommunications, computer, and high performance embedded applications, and any other application in which high speed, low latency, and scalability are necessary.

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to implement the HyperTransport communication protocol as the communication links of Kessler such that the multiprocessor system is provided with a high-speed, high-performance, point-to-point link for interconnecting integrated circuits.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Barroso discloses a multiprocessor system with an I/O card that can be seen as a processor surrogate.
- Chong discloses a multiprocessor system with an HBNS card that can be seen as a processor surrogate.
- Cronin discloses a method for terminating a processor bus.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan M. Stiglic whose telephone number is 571.272.3641. The examiner can normally be reached on Monday - Friday (6:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571.272.3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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